

TECHNOLOGY LEARNING CENTER

..Finishing School for Engineer's

VLSI MINI PROJECTS

S.NO

Projects Titles

- 1 High Speed FPGA implementation of FIR Filters for DSP Applications
- 2 Design and implementation of Floating Point Multiplier based on Vedic Multiplication Technique
- 3 A Novel Approach for parallel CRC generation FOR High Speed Application.
- 4 High speed Modified Booth Encoder multiplier for signed and unsigned numbers.
- 5 Design and Simulation of 32-Point FFT Using Radix-2 Algorithm for FPGA Implementation.
- 6 Efficient VLSI Implementation of DES and Triple DES Algorithm with Cipher Block Chaining concept using Verilog and FPGA
- 7 Implementation of an Efficient Multiplier based on Vedic Mathematics
- 8 A Floating point Fused Dot Product Unit
- 9 Implementation of Power Efficient Vedic Multiplier
- 10 LUT Optimization for Memory-Based Computation
- 11 Area Efficient parallel FIR Digital Filter Structures for Symmetric Convolution based on Fast FIR Algorithm
- 12 Measurement and evaluation of power analysis attacks on Asynchronous S-Box.
- 13 High Speed Booth Encoded Multiplier By Minimizing The Computation Time
- 14 Design Of Area Optimized AES 128 Algorithm Using Mix column Transformation.
- 15 A Secure, Low Power and Low Hardware Digital Watermarking System.
- 16 Efficient Weighted Pattern Generation Technique with Low Hardware Overhead
- 17 Low Power Design Techniques Applied to Pipelined Parallel and Iterative CORDIC Design



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- 18 Design and implementation of a high performance multiplier using HDL
- 19 A VLSI Implementation of Modulo Multiplier By Using Radix-8 Modified Booth Algorithm
- 20 Platform-Independent Customizable UART Soft-Core
- 21 A Parallel Multiplier Accumulator Based On Radix 4 Modified Booth Algorithms by Using Spurious Power Suppression Technique
- 22 Using Self-Immunity Technique 64-bit Register File Immunity Improvement
- 23 FPGA Implementation of Low power Digital QPSK Modulator
- 24 High Speed 3D DWT VLSI Architecture for Image Processing Using Lifting Based wavelet Transform
- 25 Implementation of AMBA compliant Memory Controller on a FPGA
- 26 Faster and Low Power Twin Precision Multiplier
- 27 Design and Analysis of Low Power Parallel Prefix VLSI Adder
- 28 FPGA Implementation of Booth's and Baugh- Wooley Multiplier
- 29 Implementation of Area Efficient 16bit Adder in SPARTAN-3 FPGA
- 30 Reliable and Higher Throughput Anti-Collision Technique for RFID UHF Tag
- 31 Implementation of Bus Bridge between AHB and OCP
- 32 An Implementation of Open Core Protocol for the On-Chip Bus
- 33 Implementation of OFDM System using IFFT and FFT
- 34 An Efficient FPGA implementation of Double Precision floating Point Multiplier
- 35 FPGA Based High Speed Parallel Cyclic Redundancy Check
- 36 High speed carry save multiplier based linear convolution using Vedic mathematics



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- 37 FPGA Implementation of 2-D DCT Architecture for JPEG Image Compression
- 38 Performance Evaluation of Complex Multiplier Using Advance Algorithm
- 39 Design of High Speed Vedic Square by using Vedic Multiplication Techniques
- 40 An FSM Based VGA Controller with 640×480 Resolution.
- 41 A Verilog Model of Universal Scalable Binary Sequence Detector
- 42 Hardware modeling of binary coded decimal adder in field programmable gate array
- 43 Low powers add and shift multiplier design BZFAD architecture
- 44 A High Throughput Fixed point Complex divider for FPGAs
- 45 Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics.



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