

# TECHNOLOGY LEARNING CENTER

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## B.Tech Major VLSI Project list

1. An Efficient Interpolation-Based Chase BCH decoder
2. Energy efficient code converters by using reversible logic gates
3. An efficient SQRT architecture of Carry Select adder design by Boolean algebraic equations
4. An efficient high speed Wallace tree multiplier
5. Design and implementation of 32 bit unsigned multiplier using CLAA and CSLA
6. Design of High Efficiency Carry Select Adder Using SQRT Technique
7. FPGA based implementation of a double precision IEEE floating point adder
8. LFSR-reseeding scheme for achieving test coverage
9. Optimized architecture for Floating Point computation Unit
10. Radix-4 and Radix-8 Booth Encoded Multi-Modulus Multipliers
11. Sharing Logic for Built-In Generation of Functional Broadside
12. Implementation of cryptographic algorithm on FPGA
13. 128-bit carry select adder having less area and delay
14. FPGA implementation high speed vedic multiplier using barrel shifter
15. Improved Design of Low Power TPG Using LPLFSR
16. HICPA:64 bit hybrid low power adder for high performance processors
17. 128 bit low power VLSI adder subsystem
18. Parity preserving logic based fault tolerant reversible ALU.
19. Efficient concurrent BIST with comparator based response analyzer
20. Area efficient high speed low power multiplier architecture for multirate filter design
21. Used self controllable voltage level techniques to reduce leakage currents in DRAM 4\*4 in VLSI
22. Minimization leakage current of full adder using deep sub micron CMOS technique
23. Normaliation of floating point multiplication using verilog hdl



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24. Design and implementation of truncated multipliers for precision improvement and its application to a filter structure
25. Design of high speed hardware efficient 4 bit sq multiplier
26. Hdl implementation of non restoring division algorithm using high speed adder or subtractor
27. Implementation of fixed point square root algorithm on fpga hardware
28. Platform independent customizable UART soft core
29. Design and Implementation of FPGA based High Resolution Digital Pulse Width Modulator Resolution Digital Pulse Width Modulator
30. Design and implementation of floating point ALU in FPGA
31. Hardware implementation of truncated multiplier based on multiplier usingFPGA
32. Time multiplexed offset carrier QPSK for GNSS.
33. GF(Q) LDPC decoder design for FPGA implementation
34. A high speed and low power VLSI multiplier using redundant binary booth encoding
35. FPGA implementation of booths and baugh wooley multiplier using verilog
36. RTL design and implementation of BPSK modulation at low bit rate
37. Architecture and implementation of a vector/SIMD multiply accumulate unit
38. 32 bit MAC unit design using vedic multiplier
39. Design and implementation of truncated multiplier for precision improvement
40. Low transition LFSR for bist based application
41. Arbitary density pattern based reduction of testing time in scan-bist VLSI circuits
42. Low Power 10-Transistor Full Adder Design Based on Degenerate Pass Transistor Logic
43. Design of 64-Bit Low Power Parallel Prefix VLSI Adder for High Speed Arithmetic Circuits
44. Design of low power high speed vlsi adder Subsystem
45. Synthesis and Implementation of UART using verilog Codes
46. HICPA: A Hybrid Low Power Adder for High-Performance Processors



47. Low-Power and Area-Efficient Carry Select Adder
48. Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics
49. Design and Implementation of a High Performance Multiplier using HDL
50. design of low-power and high performance radix-4 multiplier
51. CORDIC Designs for Fixed Angle of Rotation
52. High Speed and Area Efficient Vedic Multiplier
53. Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure
54. Low power variation aware flipflop
55. High speed Modified Booth Encoder multiplier for signed and unsigned numbers
56. An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform
57. High Speed Signed Multiplier for Digital SignalProcessing Applications
58. Accumulator Based 3-Weight Pattern Generation
59. Design of Low Power TPG Using LP-LFSR
60. A Real-time Face Detection And Recognition System
61. Verilog Implementation of UART with Status Register
62. FPGA Based Real Time Face Detection using Adaboost and Histogram Equalization
63. Design and Implementation of Area-optimized AES
64. Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure
65. A distributed canny edge detector and its implementation on fpga
66. An Efficient Implementation of Floating Point Multiplier
67. Design and Simulation of UART Serial Communication Module Based on verilog
68. Design and VLSI Implementati on of High-Performance Face-Detection Engine for Mobile Applications
69. Design and Implementation of Area-optimized AES Based on FPGA
70. High Speed ASIC Design of Complex Multiplier Using Vedic mathematics.
71. A New Reversible Design of BCD Adder.



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72. Parallel Architecture for Hierarchical Optical Flow estimation
73. A Very Fast and Low Power Carry Select Adder Circuit
74. Design and Characterization of Parallel Prefix Adders using FPGA.
75. FPGA based FFT Algorithm Implementation in WiMAX Communications System
76. A FPGA Design of AES Core Architecture for Portable Hard Disk
77. FPGA Implementation of RS232 to Universal serial bus converter
78. Image Encryption Based On AES Key Expansion
79. FPGA Implementation of AES Algorithm
80. Design of Serial Communication Interface Based on FPGA
81. Design and Implementation of an FPGA-based Real-Time Face Recognition System
82. Design enhancement of combinational neural networks using hdl based fpga
83. Efficient VLSI Architecture for Discrete Wavelet Transform



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